

FIG. 1

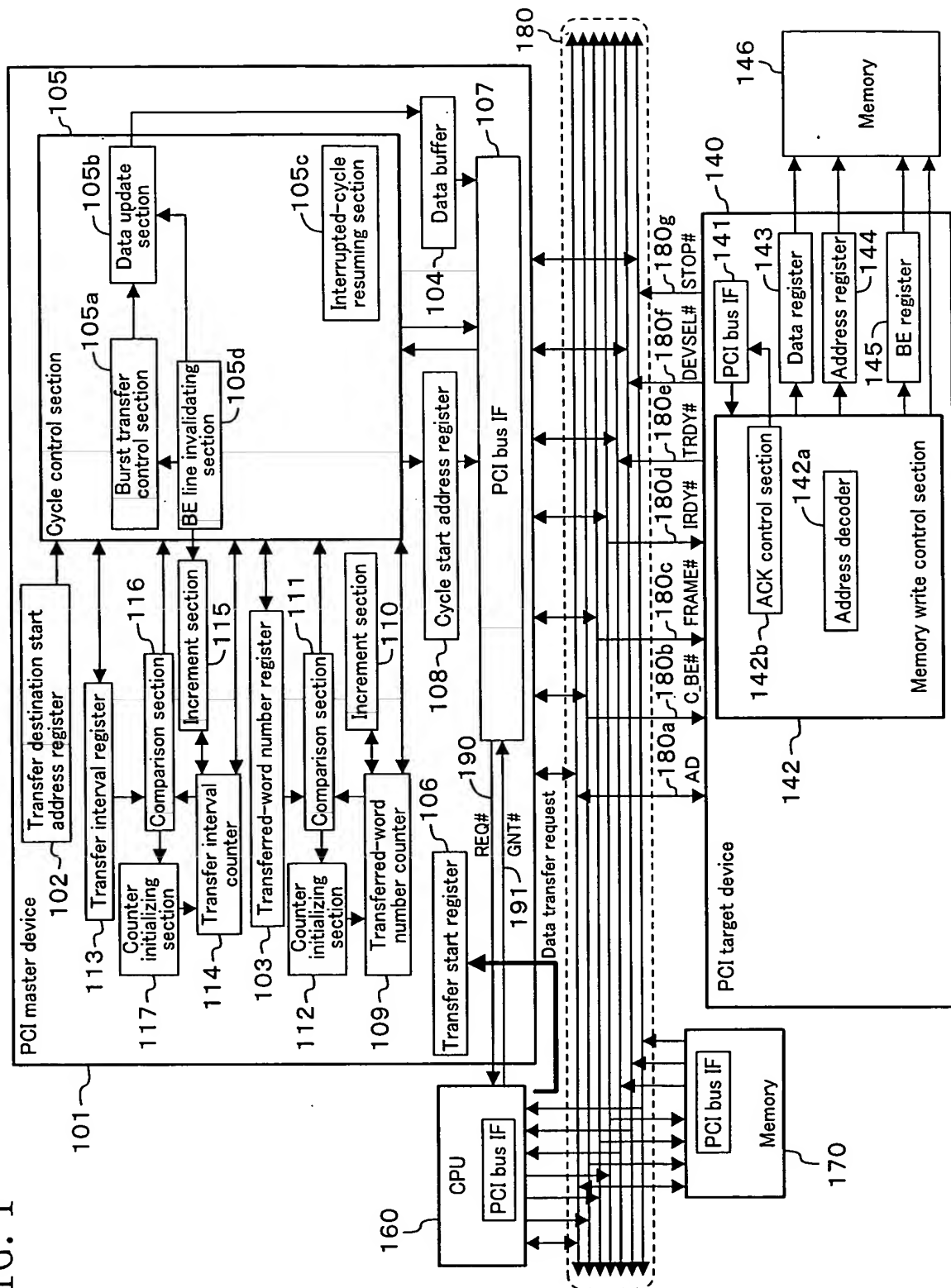


FIG. 2

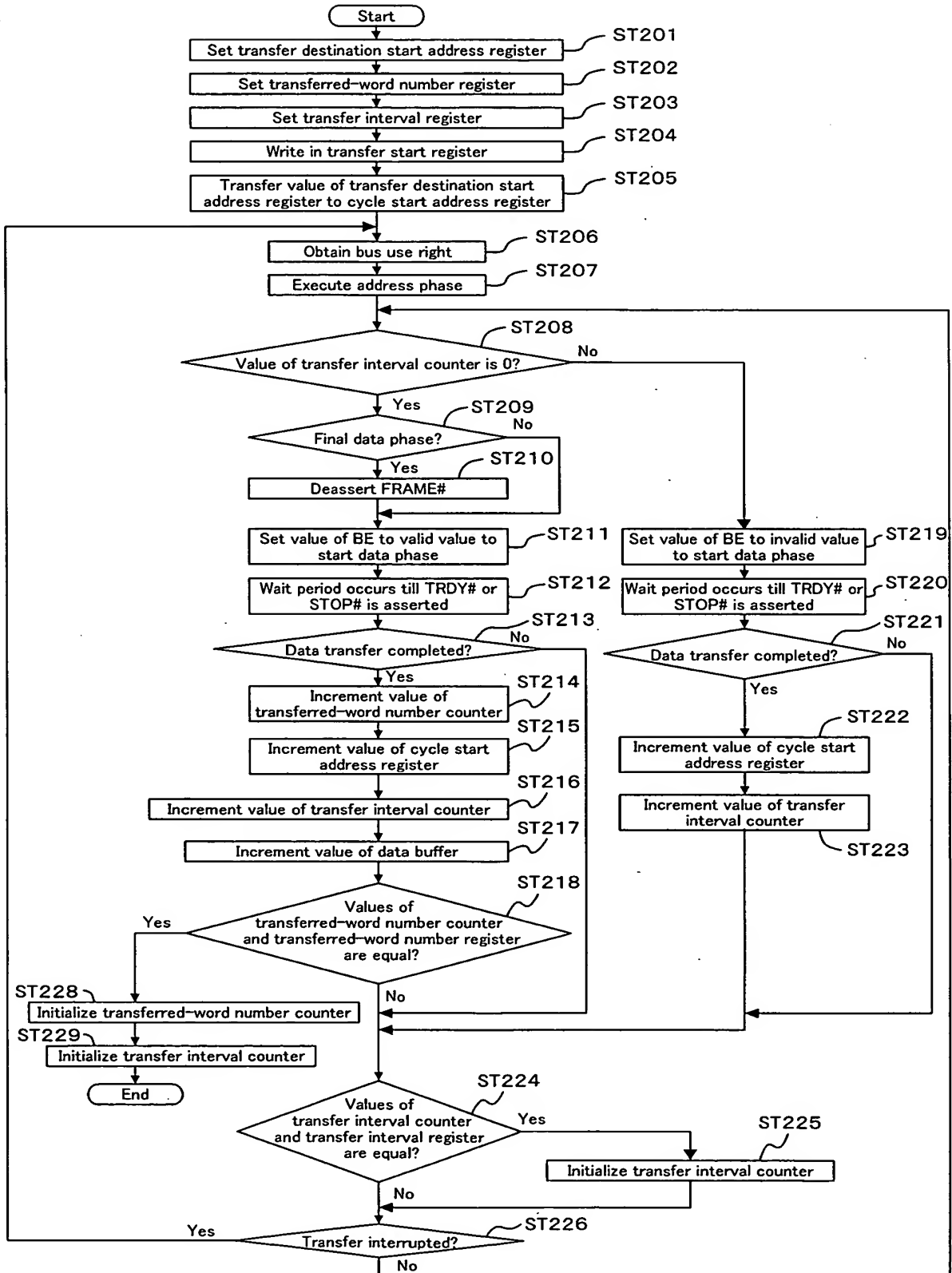


FIG. 3A

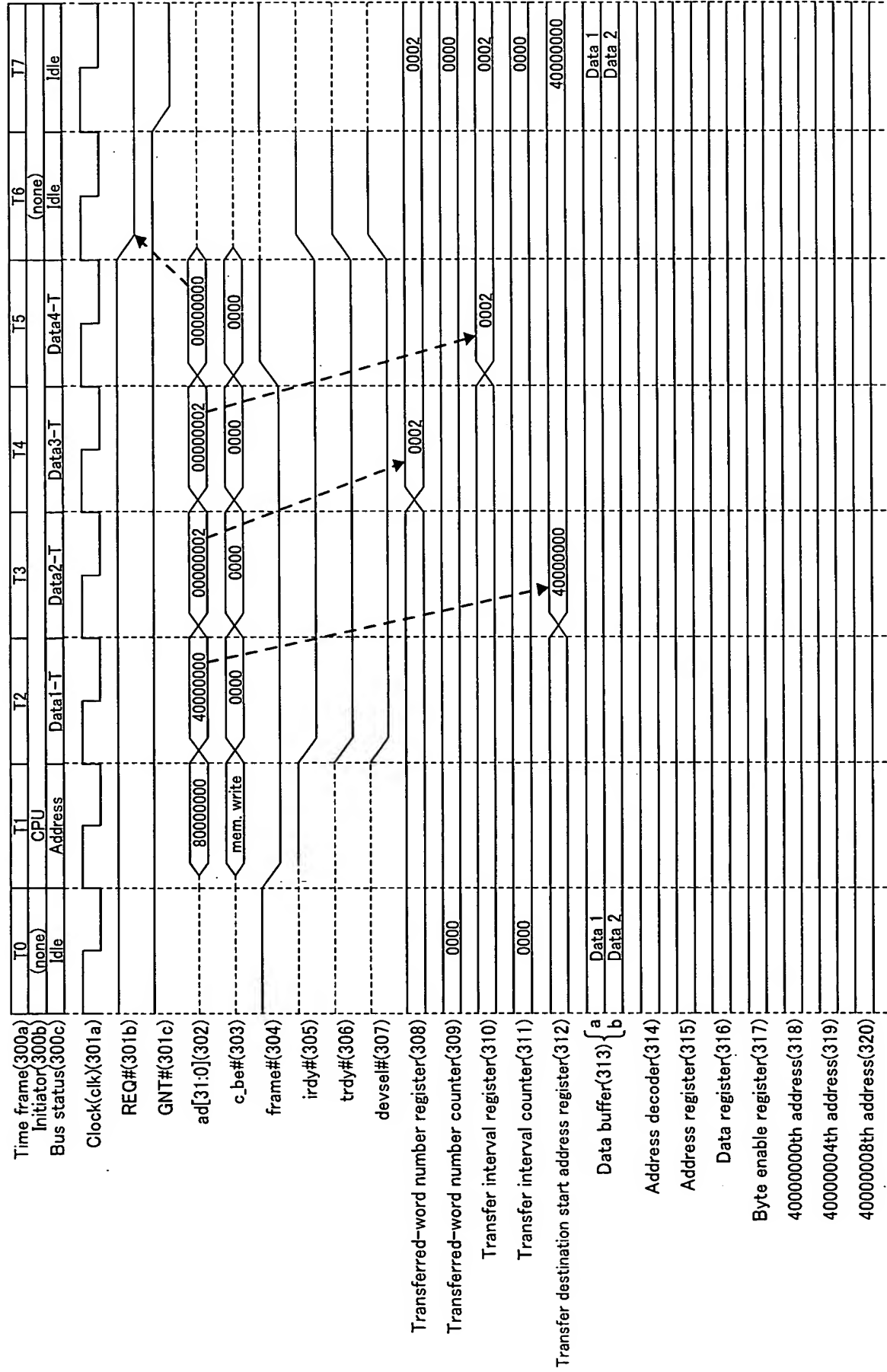


FIG. 3B

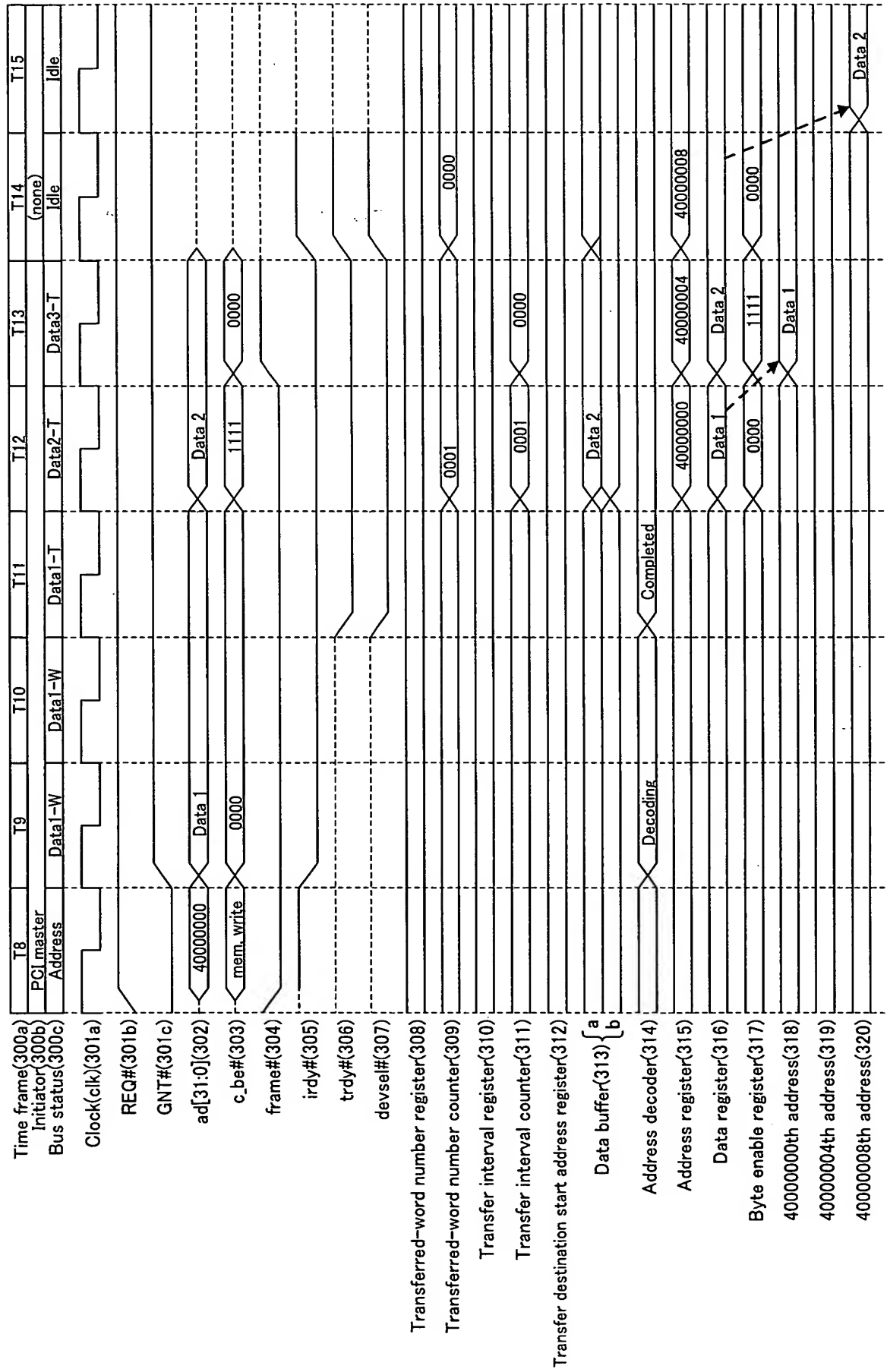


FIG. 4

Start address	End address	allocated to:
00000000	3ffffff	Memory 170
40000000	7ffffff	Memory 146
80000000	80000003	Transfer destination start address register 102
80000004	80000007	Transferred-word number register 103
80000008	8000000b	Transfer interval register 113
8000000c	8000000f	Transfer start register 106

FIG. 5

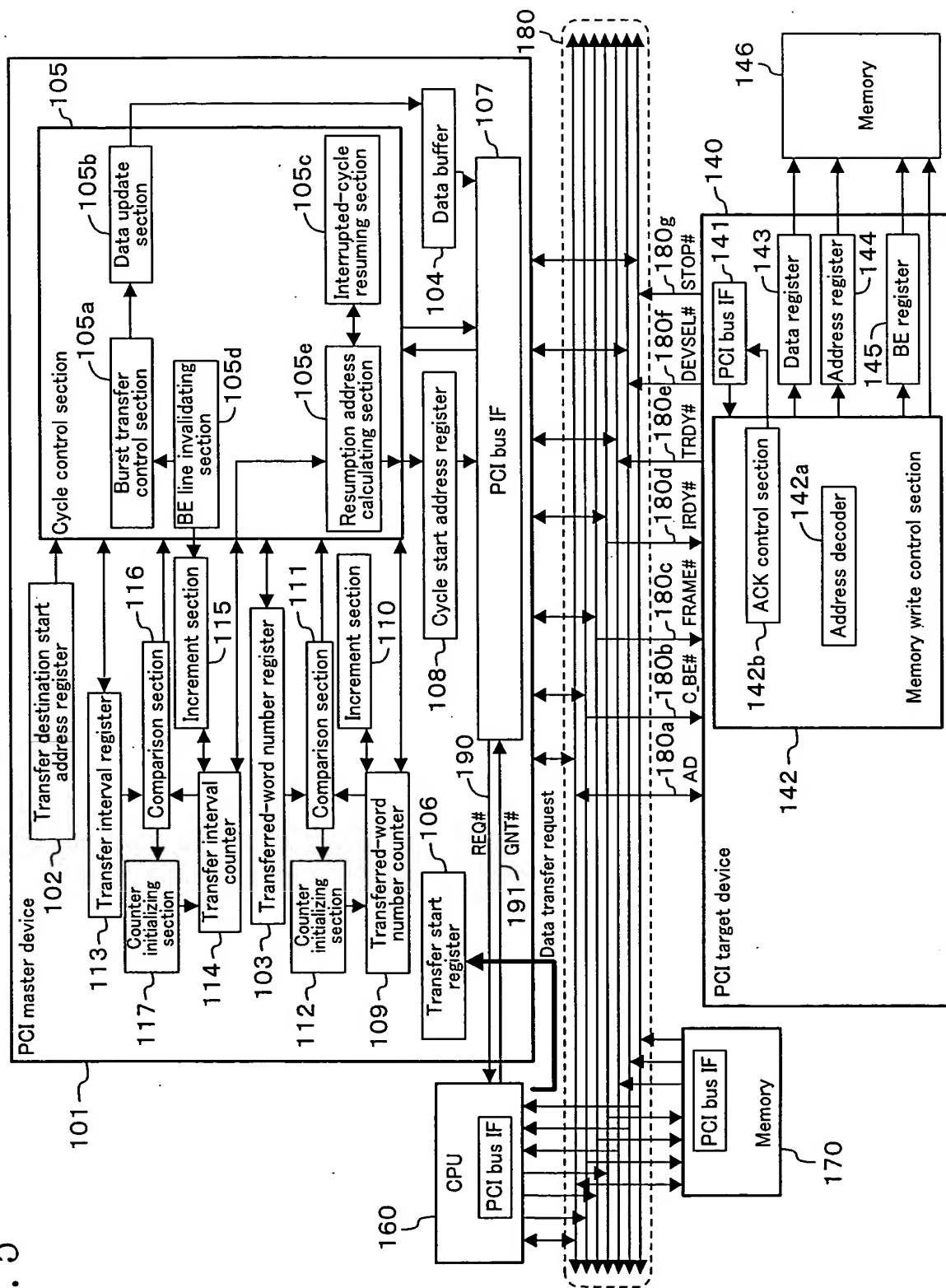


FIG. 6

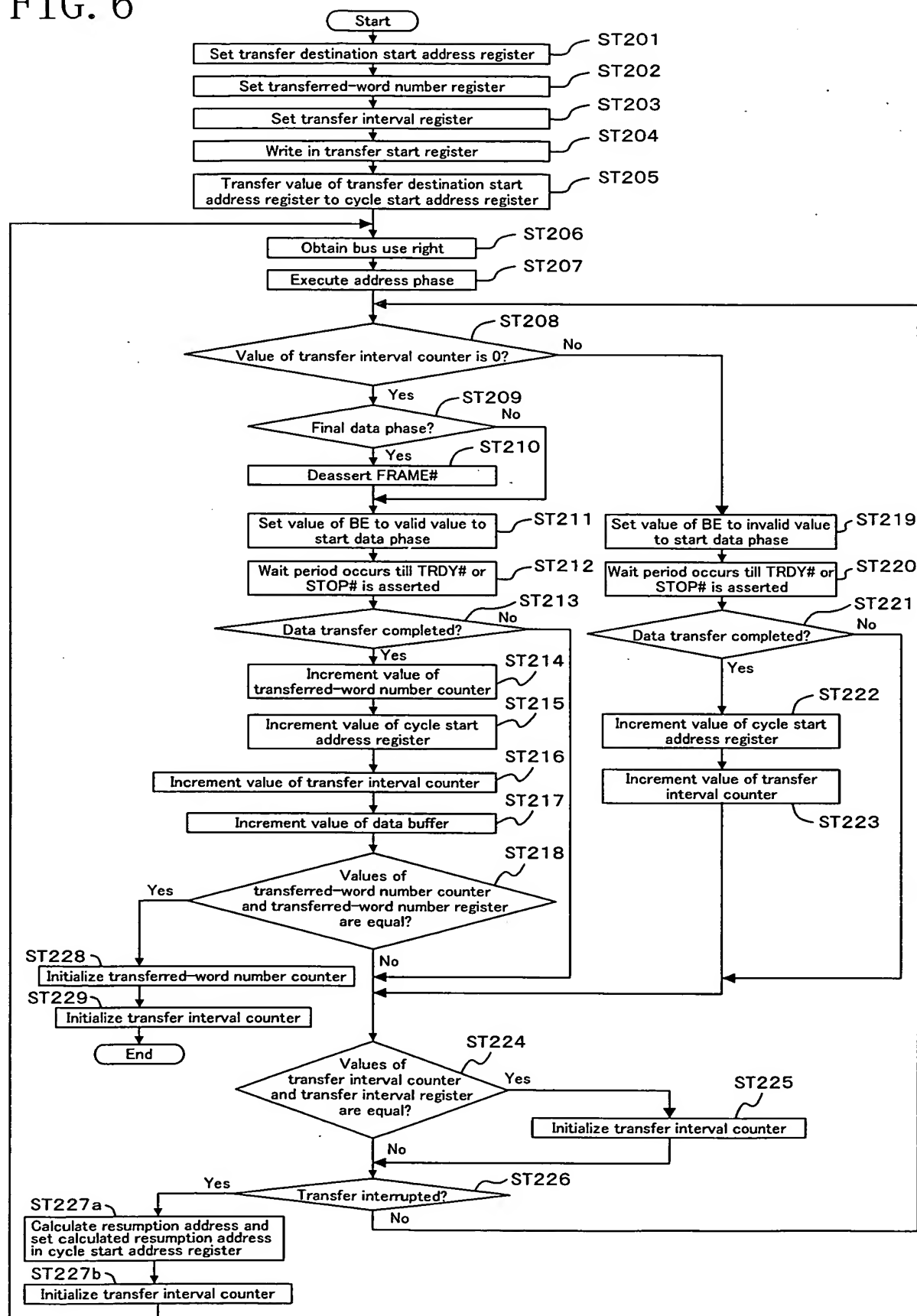


FIG. 7

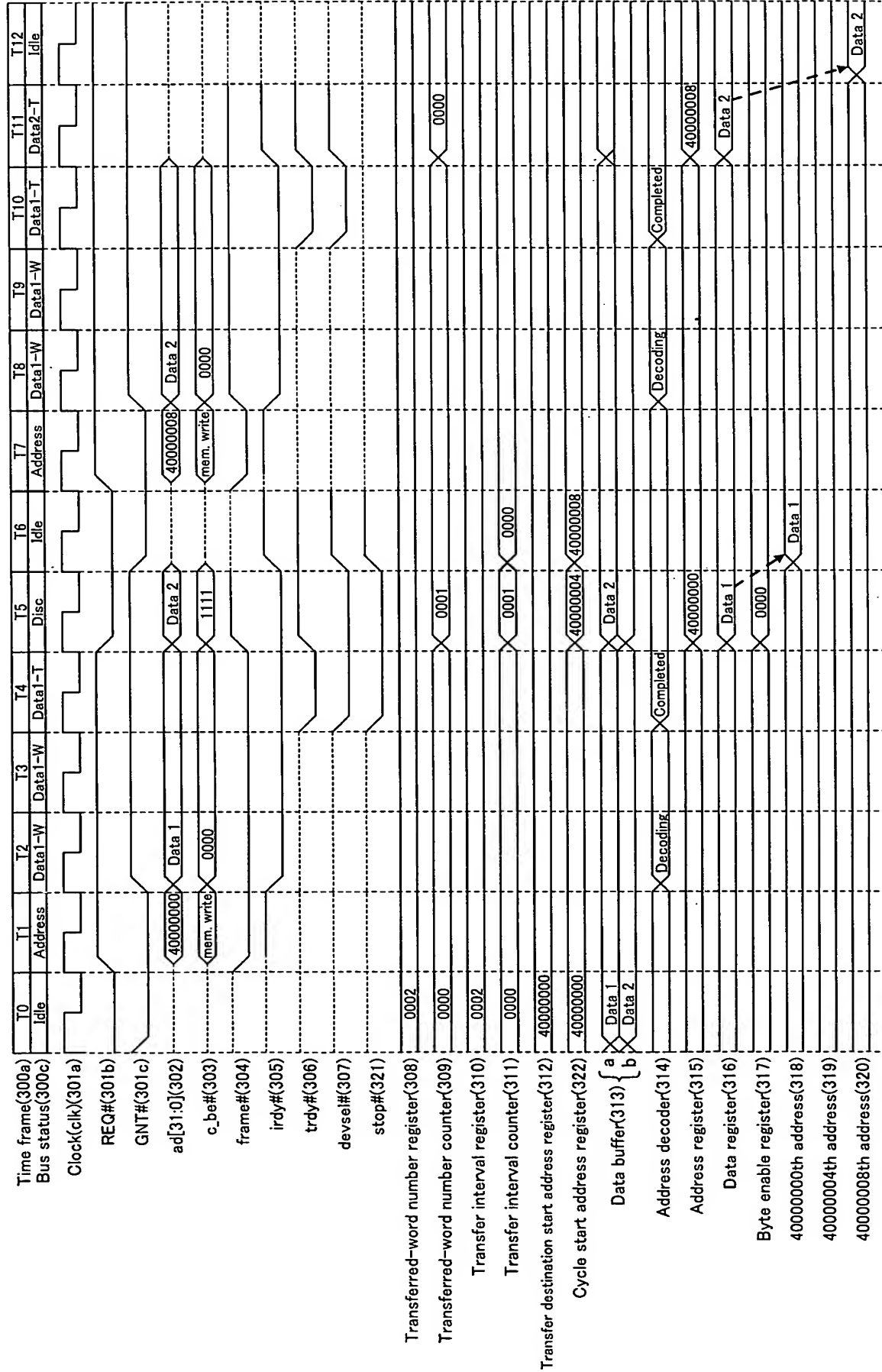




FIG. 8A

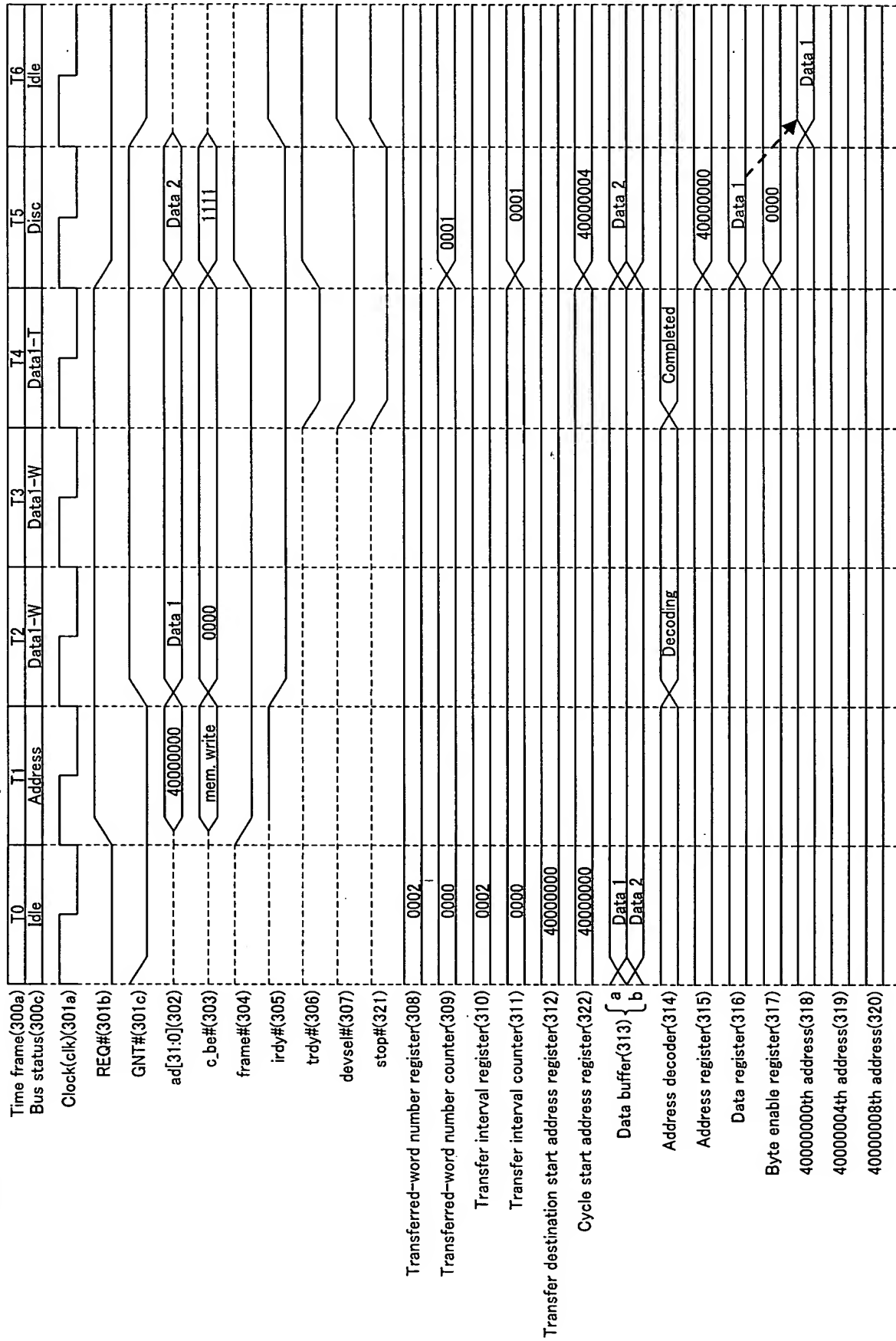


FIG. 8B

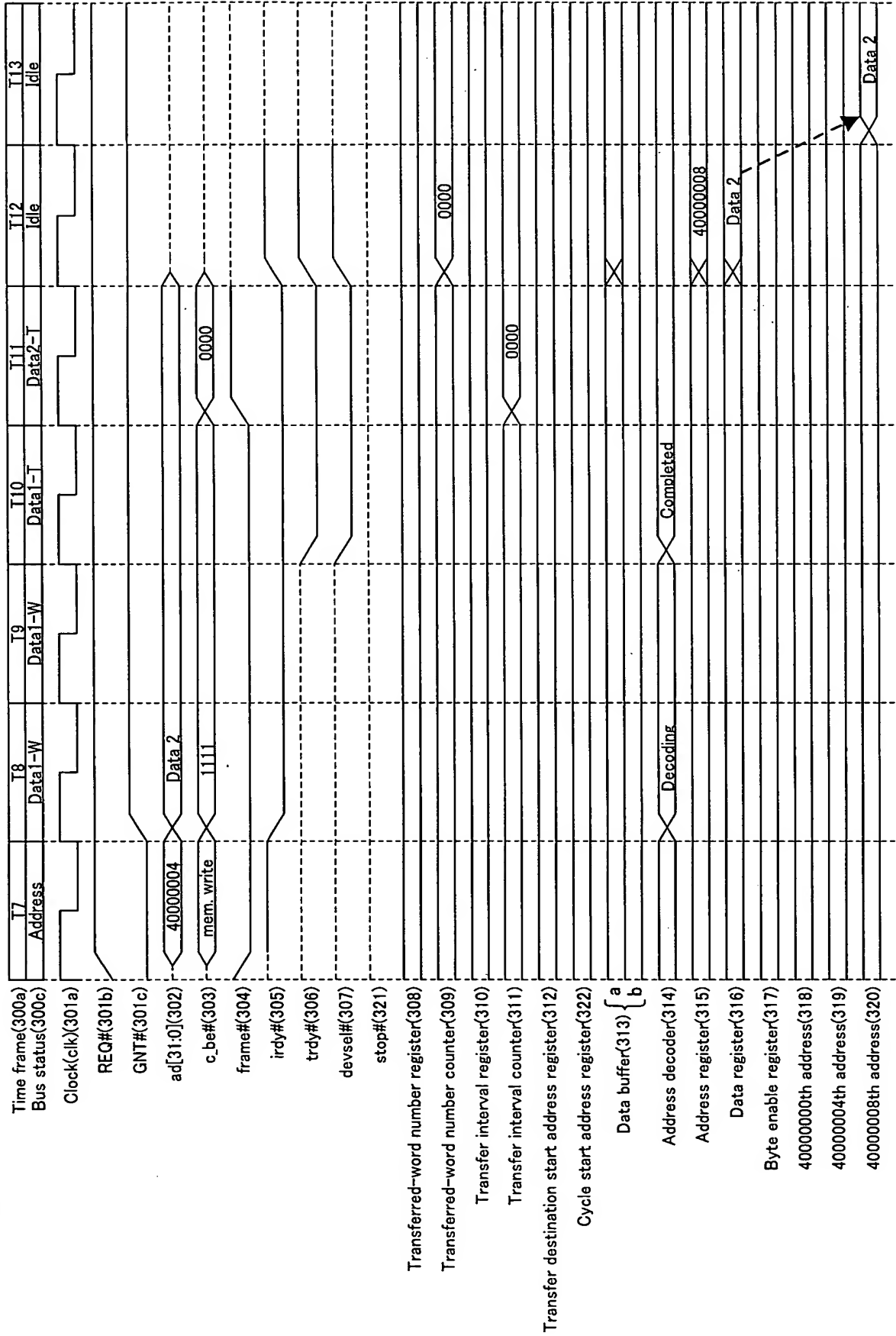


FIG. 9

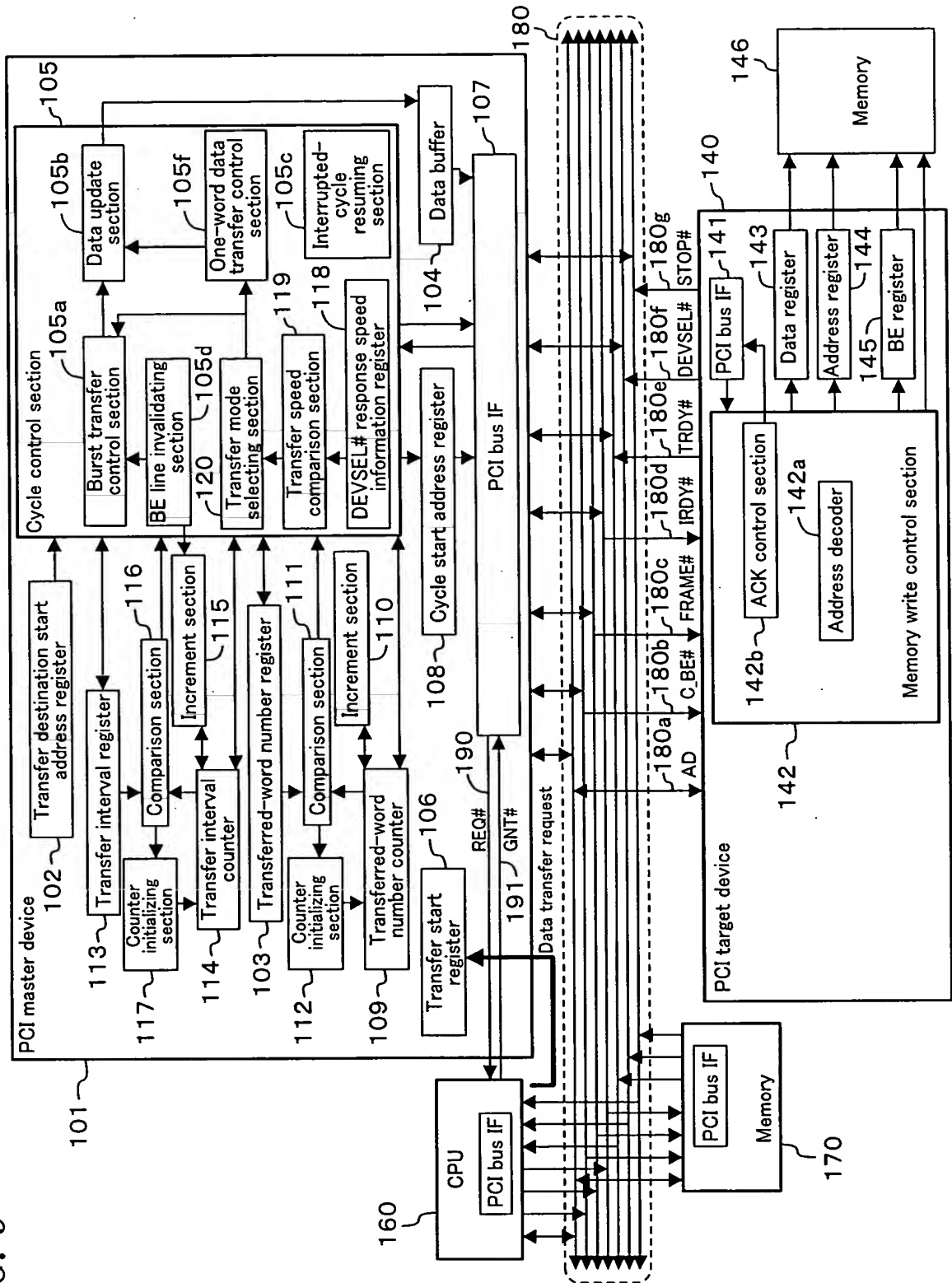






FIG. 12

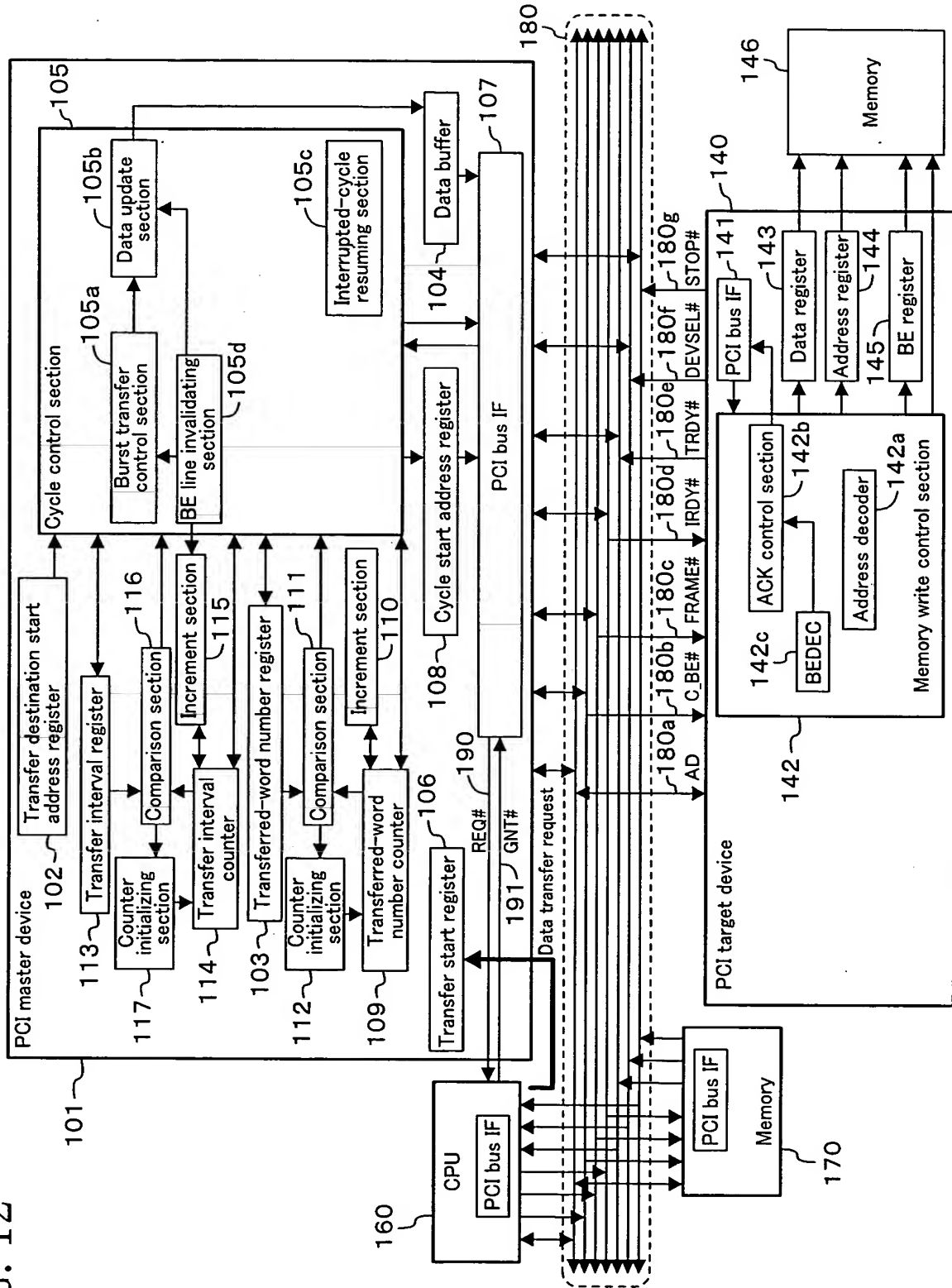


FIG. 13

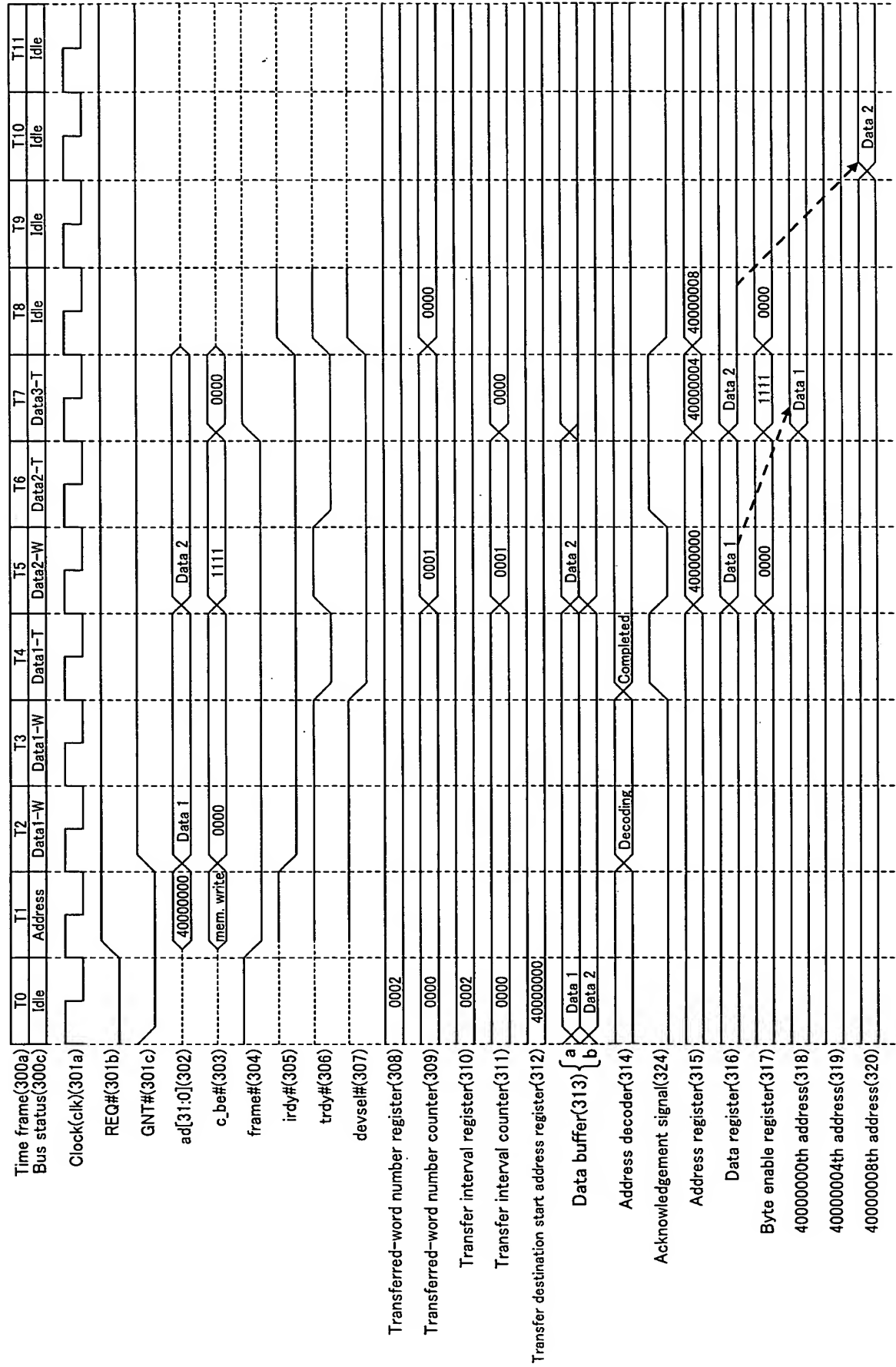






FIG. 15

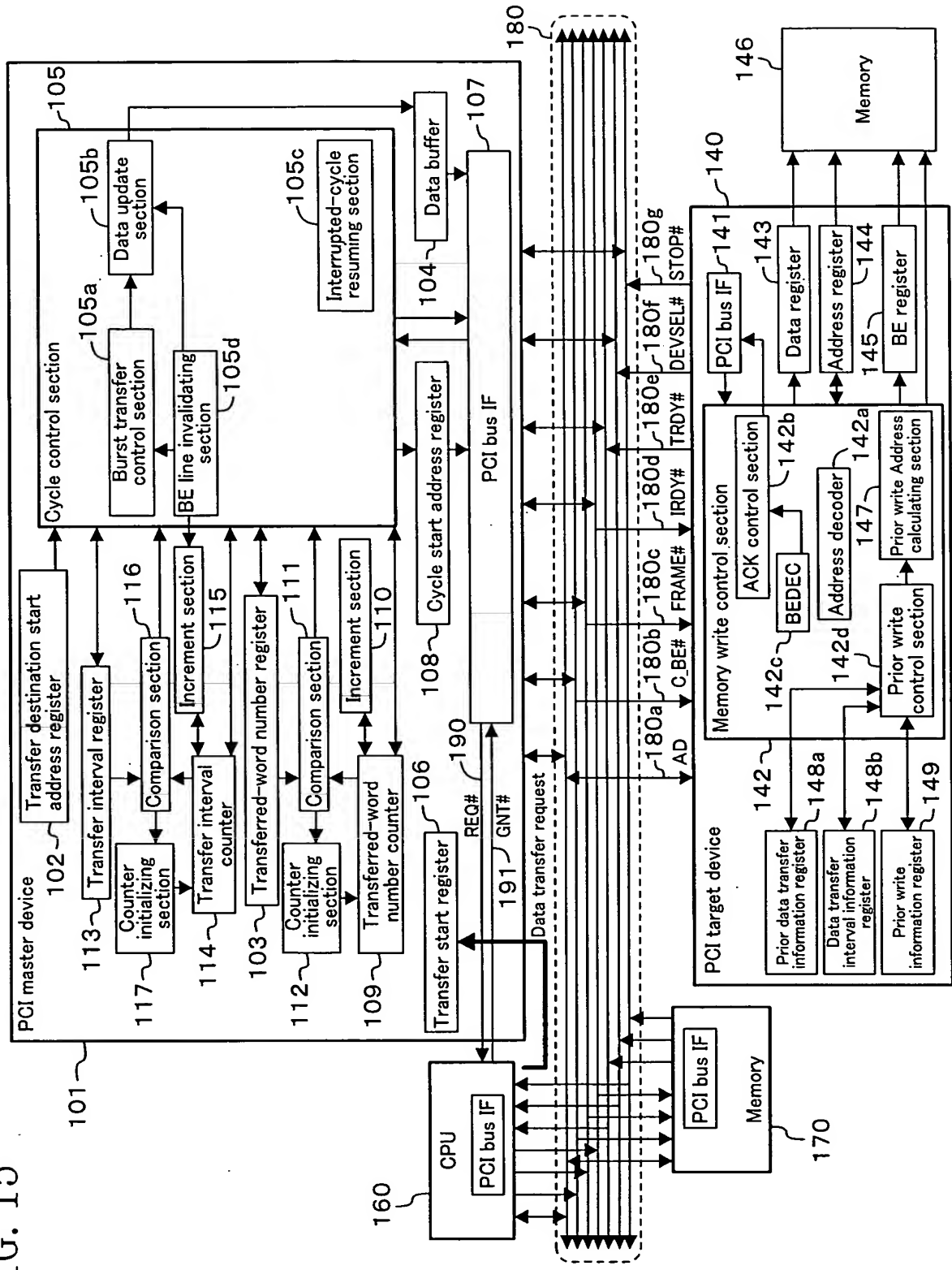




FIG. 17

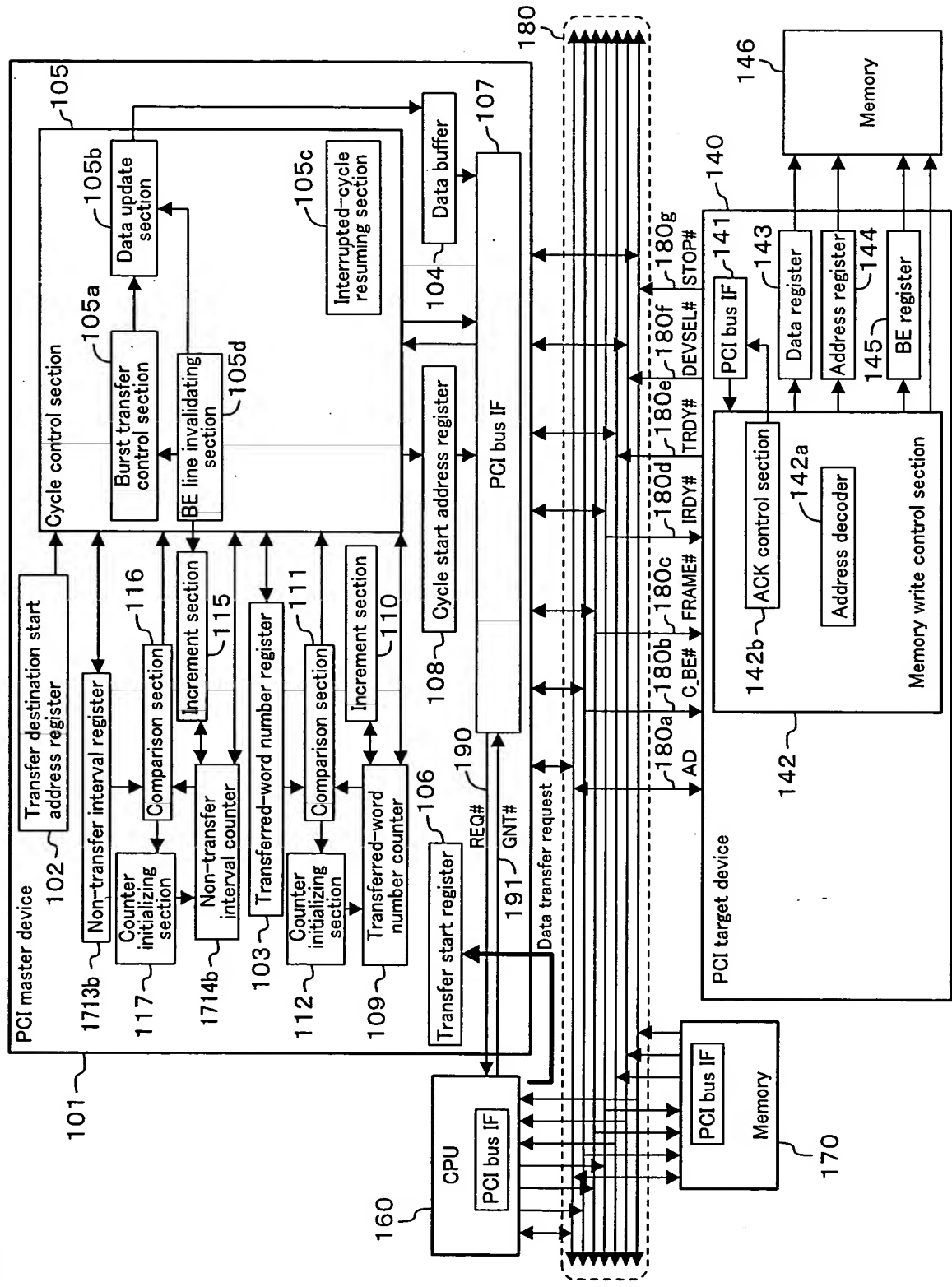


FIG. 18

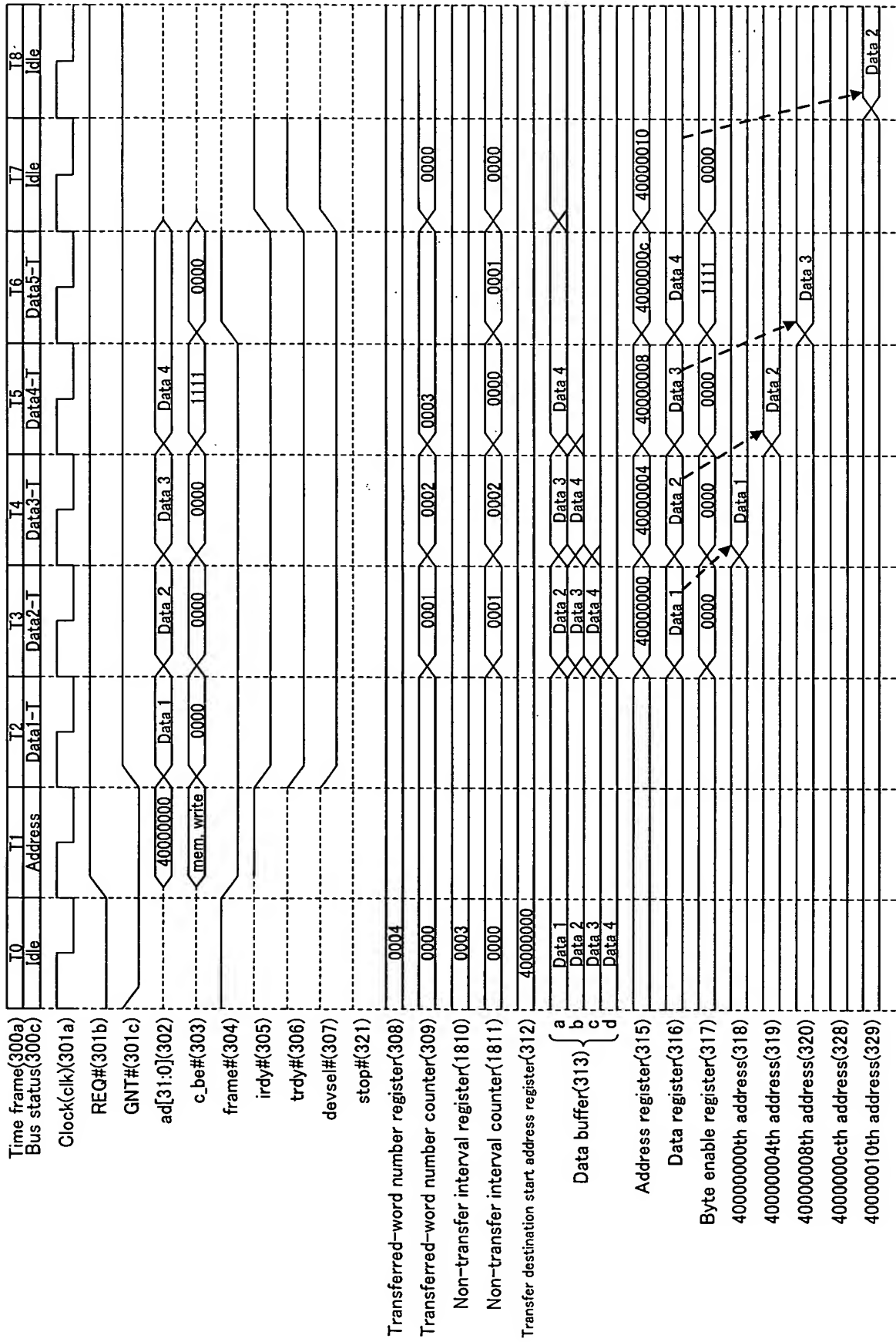


FIG. 19

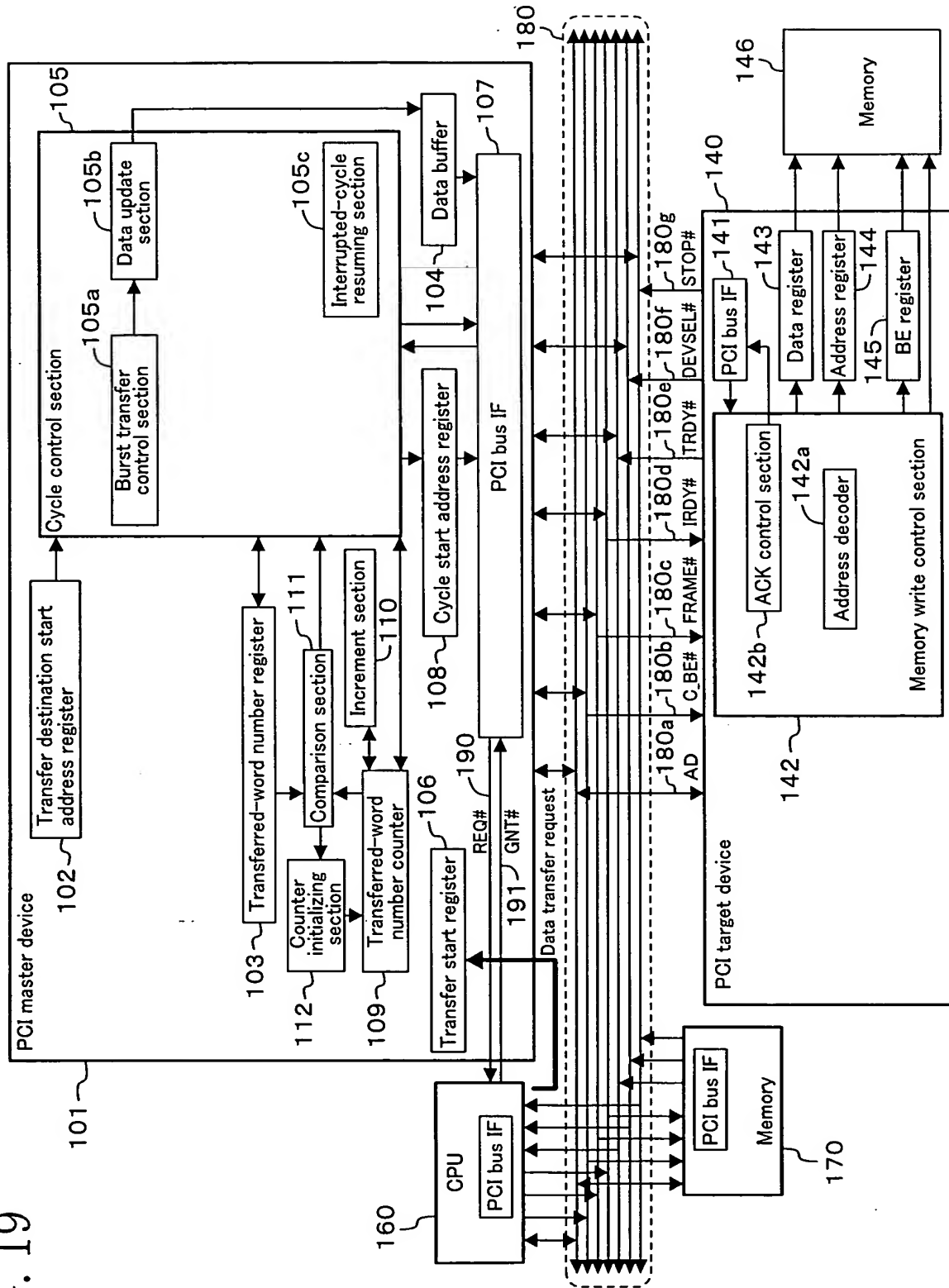




FIG. 20B

